ORIGIN OF OPEN CIRCUIT VOLTAGE LIMIT FOR TRANSFER SOLAR CELLS

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ABSTRACT: The transfer process invented and developed at *ipe* enables the fabrication of 50 μm thin monocrystalline silicon solar cells with efficiencies up to 17.0 %. Simulations as well as cells fabricated on thinned wafers with thicknesses of 50 μm show an efficiency potential above 21 %. In the past much research work concentrated on the back side passivation due to the fact that thin solar cells are more affected by back side recombination. However, back side passivation of transfer cells shows a limited open circuit voltage of 630 mV. In contrast, using the same passivation on wafered material, we achieved an open circuit voltage of 670 mV. This contribution shows that the limitation of the open circuit voltage of transfer cells is due to platinum contamination, which stems from one step used in the transfer process, namely porous silicon fabrication. Simulations predict open circuit voltage up to 700 mV by suppressing the Pt contamination at back side recombination velocity of 100 cm/s.

Keywords: Thin film, silicon, solar cells, recombination via traps

1 INTRODUCTION

The reduction of the solar cell thickness decreases the material consumption, offers the fabrication of mechanically flexible cells, and enhances the physical properties of solar cells such as increasing the open circuit voltage. Just reducing the thickness of the fabricated wafer during ingot slicing is obviously not sufficient, as material losses will remain a factor for silicon wastage. To avoid the silicon wastage, the *ipe* has invented and developed the transfer layer process [1, 2]. The transfer process is based on the epitaxial growth of monocrystalline silicon on the top of thermally restructured double porous silicon layers. Porous silicon forms by electrochemical etching a silicon wafer in aqueous hydrofluoric acid solution using platinum electrodes. Platinum is chosen because of its high stability in hydrofluoric acid. The transfer process provides an economical production of high quality monocrystalline thin silicon solar cells with thicknesses between 20 and 50 μm either on a foreign substrate [1, 3, 4] or free standing [5-7]. The best efficiency of a transfer cell with a thickness of 50 μm is 17.0 %. In fact, solar cells with small thicknesses are affected by the recombination at the back side more than thick cells. Therefore, passivating the back side should increase the open circuit voltage and hence the cell performance. Brendle [8] developed a novel low temperature back side passivation, which showed open circuit voltage V_{oc} = 670 mV for wafer based cells. Unfortunately, the same passivation of the back side enhances the open circuit voltage V_{oc} of transfer cells from V_{oc} = 630 to only V_{oc} = 640 mV. This result leads us to the idea that the limiting mechanism of the transfer solar cells is not the back side, as thought by many other authors, but a process which is related to the production of the thin layers.

The present contribution shows platinum contamination during porous silicon etching to be responsible for the open circuit voltage limitation of transfer solar cells. The platinum contamination of etched wafers on both sides is proven by secondary ion mass spectroscopy (SIMS) measurements. The platinum forms deep energy level E_{pt} = 0.37 eV in the silicon band gap measured from the conduction band edge [9]. The simulation shows that this deep level leads to an effective minority carrier diffusion length L_{eff} = 120 μm, which is the same determined value as from the internal quantum efficiency analysis of the best transfer cell [5, 6]. This means, passivating the back side without suppressing the platinum contamination is not useful to enhance the performance of the transfer cells. First, a new method must be found to avoid the platinum contamination during porous silicon formation. One possibility is to use graphite or silicon electrodes.

2 EXPERIMENTAL DETAILS

The transfer layer process [1, 2] produces thin silicon films in three steps. First, hydrofluoric (HF) acid electrochemically etches pores into a silicon host wafer and prepares the wafer for the transfer process. Second, epitaxy grows thin monocrystalline silicon on the etched and restructured porous silicon. In a third step, the thin silicon layer is separated from the host wafer and serves as a wafer equivalent for solar cell fabrication.

Figure 1 schematically describes the etching cell for porous silicon etching. A double chamber cell structure filled with aqueous HF solution enables the back side contacting of the host wafer without a direct contact to the platinum anode. Cathodic attack etches porous silicon on the front side of the wafer. A high concentration of HF is selected to enhance the back contact as well as to optimize the porosity [3, 7]. A low etching current creates an upper low porosity layer of a thickness of 1.2 μm and porosity between 20 and 30 %. Increasing the etching current for a short time, builds a 300 nm thin buried high porosity layer with porosity between 50 and 60 %. A high temperature treatment at T = 1050 °C in hydrogen atmosphere restructures the double layer porous silicon system. The upper layer serves as a seed for a high quality epitaxy layer growth. The lower layer transforms to a buried cavity with some remaining silicon bridges, which enables a stable system while solar cell processing and the separation of the epitaxy layer afterwards.

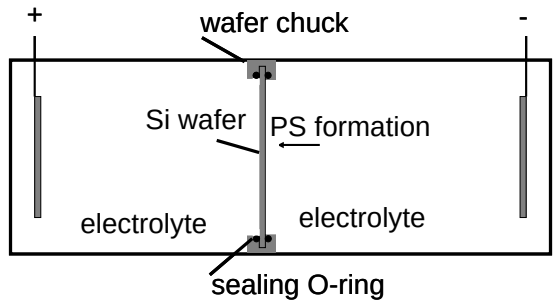

Figure 1: Double chamber etching cell for porous silicon fabrication. An O-ring sealing fixes the wafer from both sides. The electrodes consist of platinum.

Figures 2 a, b show a cross sectional scanning electron micrograph (SEM) of the wafer edge after the epitaxy in two positions. The etching parameters are adjusted [4, 7] in order to create a continuous buried cavity everywhere beneath the epitaxy layer except at the edges of the wafer, where the O-ring sealing are positioned.

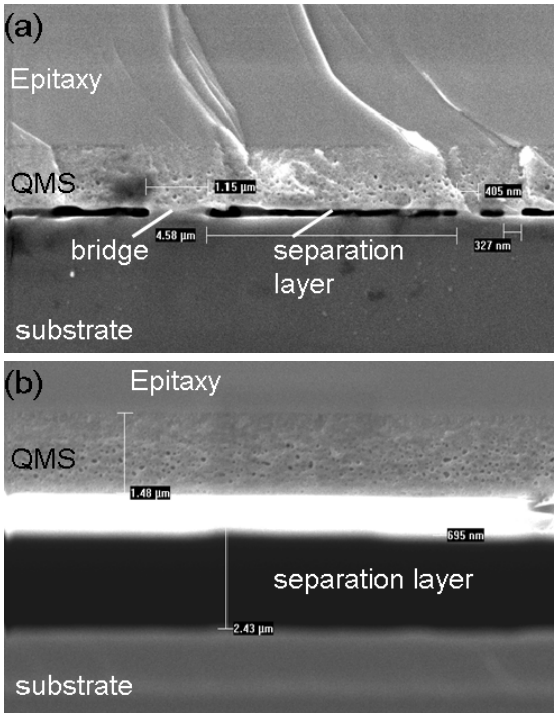

Figure 2: Scanning electron microscope (SEM) pictures of the cross section of wafer after epitaxy growth at (a) the location of the O-ring and (b) in a location inside the wafer away from the edge. The silicon bridges at the edge enable the structure fixation during cell processing. The continuous cavity beneath the epitaxy layer provides easy separation of the fabricated device.

Figure 2a shows that the separation layer at the location of the O-ring sealing is interrupted by silicon bridges. The quasi-monocrystalline silicon (QMS) layer on the back side of the epitaxy layers causes high charge carrier recombination due to the large internal area and the high doping density. Figure 2b depicts the continuous separation layer between the host wafer and the epitaxy layer, which enables the easy separation of the fabricated device. Device fabrication starts with the layer system still attached to the wafer. The solar cell front side is textured with random pyramids by KOH. A thermal silicon dioxide layer is formed on a low n-type doped emitter with a sheet resistance ρ_{em} = 100 Ω/□ and acts as passivation and anti-reflection coating (ARC) layer. Titanium, palladium and silver are evaporated and patterned as a front contact grid by using photolithography and lift-off processes. The back contact is formed by Al evaporation after the cell separation from the host wafer by mechanical force using a vacuum pick-up system. Cells with back side passivation have a different back side processing as described in Ref. [8]. The QMS layer is first chemically etched and the back side is passivated using a system of a-Si:H/a-SiN_x:H/Al and the contacts are formed locally by laser firing.

3 RESULTS AND DISCUSSIONS

Figure 3 depicts the platinum depth profile measured by secondary ion mass spectroscopy (SIMS) at the back side of a silicon wafer after porous silicon etching. The platinum depth profile shows a surface concentration of $N_{pt,s} = 3\times10^{21}$ cm^{-3} and a depth d_{pt} = 200 nm. We ascribe the platinum contamination to the electrochemical deposition during porous silicon etching, while the wafer back side behaves as a cathode with respect to the etching cell anode.

After epitaxy growth SIMS measurements show no platinum contamination. We ascribe this finding to two factors: First, the Platinum contamination redistributes during the high temperature processing steps throughout the 50 µm epitaxy layer and the wafer. This effect results in a net Pt concentration beneath the SIMS detection sensitivity $N_{lim} = 2\times10^{19}$ cm^{-3}. Second, porous silicon beneath the epitaxy layer getters the platinum contamination.

The worst case scenario is the total amount of the Platinum depth profile to be redistributed throughout the epitaxy layer only. This estimate results in an average Pt distribution $N_{pt,av} = 2\times10^{17}$cm^{-3}, which is below the SIMS sensitivity by two orders of magnitude. This result supports the first assumption that platinum redistributes through the sample. The Pt contamination vanishes from SIMS measurements after epitaxial deposition on the QMS layer on the back side of a transferred thin film as well as on the front side of the wafer. Thus, instead of porous silicon gettering the platinum contamination a redistribution throughout the wafer has taken place. In the following we assume an epitaxy layer with a platinum contamination of up to $N_{pt,av} = 2\times10^{17}$cm^{-3}.

The platinum forms deep energy levels at E_{pt} = 0.37 eV in the silicon band gap measured from the conduction band edge, with a capture cross section $\sigma_{pt} = 1.1\times10^{14}$cm^2 [9]. Calculations based on Shockley-Read-Hall recombination model [10] lead to an effective minority carriers diffusion length L_{eff} = 120 µm, which agrees with the value which we derived from internal quantum efficiency analysis of the best transfer cell [5, 6].

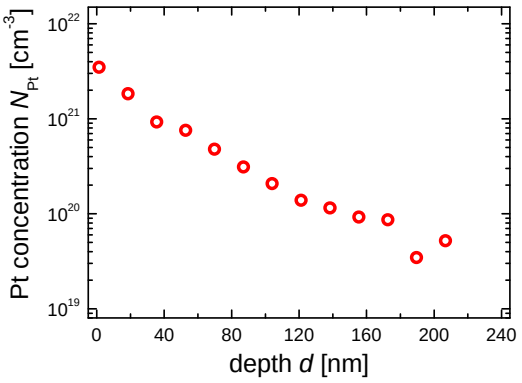

Figure 3: Depth profile of platinum measured by secondary ion mass spectroscopy at the wafer surface after porous silicon etching. Platinum electrochemically deposits on the wafer surfaces during porous silicon formation.

Figure 4 shows the calculated open circuit voltage V_{oc} for 50 µm thin solar cells as a function of the platinum concentration for different back surface recombination velocities S_b. A platinum concentration $N_{pt,av} = 10^{14}$ cm^{-3} leads of $V_{oc} \approx 600$ mV regardless of the back side passivation quality. To see the effect of the back side passivation, the platinum concentration should be below $N_{pt} = 10^{13}$ cm^{-3} and $\Delta V_{OC} = 10$ mV enhancement could be achieved if $N_{pt} < 10^{12}$ cm^{-3}.

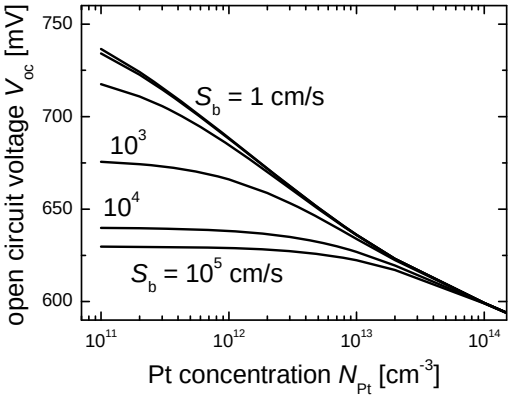

Figure 4: Calculated open circuit voltage for 50 µm thin solar cells as for different back surface recombination velocities S_b. Back surface passivation has no significant enhancement of the cell performance at platinum concentrations $N_{pt} > 10^{13}$ cm^{-3}.

5 CONCLUSIONS

This paper has shown that the real limit of the transfer solar cell performance is not the back side recombination losses, as thought by other authors. Instead the main limiting mechanism lies in a Pt-contamination which leads to bulk recombination. Prior to enhancing the back side passivation, the platinum contamination must be suppressed. The use of graphite or silicon electrodes during porous silicon formation possibly serves this purpose

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