Compact Modeling of CMOS Transistors under Uniaxial Stress

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***Abstract*—Changes in the BSIM3 compact model are necessary in order to accurately simulate the CMOS transistors under applied uniaxial stress. In this paper we focus on the analysis of external uniaxial mechanical stress effects on DC BSIM3 model parameters of bulk MOS-FETs fabricated in a $0.8\mu m$ CMOS process. The results show that stress influences mostly the carriers mobility while the threshold voltage remains almost unchanged. We measured the piezoresistive coefficients for different transistor geometries and used them to adjust the BSIM3 mobility parameter in order to include stress effects. Moreover, we propose a modified MOS-FET circuit able to simulate the transistor under variable uniaxial stress conditions. The simulation results were compared with the experimental ones and found to be in good agreement.**

***Index Terms*—BSIM3 model, flexible electronics, piezoresistivity, strained-Si, uniaxial stress.**

I. Introduction

Deformation induces stress in the chip that leads to the piezoresistive effect. The applied mechanical stress changes the electrical characteristics of MOS-FETs. Therefore, the transistor characteristics will no longer be static but vary with the applied stress.

The standard MOS transistor models BSIM3, for circuit simulation programs such as SPICE, does not include any stress effects. Therefore, it can not correctly predict the circuit performance under variable applied mechanical stress, leading to inprecise simulations. To accurately simulate the CMOS circuits under variable stress, the piezoresistive effect needs to be considered in MOS-FET design.

In this work we analyze the effect of applied uniaxial stress on the MOS-FET DC BSIM3 model parameters. Further we change the mobility model parameter based on its measured sensitivity to the applied stress. An equivalent MOS-FET circuit able to simulate variable stress effects is introduced. The simulation results of n- and pMOS transistors based on the modified parameters are then discussed and compared with the measured data.

The paper is structured as follows: in Section II we introduce the measured transistors and the bending method. In Section III we analyze the variation of mobility and threshold voltage BSIM3 model parameters under uniaxial stress. Further on, in Section IV we propose an equivalent circuit for NMOS-FET and in Section V we present the simulation results. Finally, we end this paper in Section VI with a brief conclusion and ideas for future work.

II. Experiments

A. Tested Devices

n- and pMOS bulk transistors were fabricated on (001) silicon substrates using an in-house IMS $0.8\mu m$ CMOS process. After the fabrication, we sawed the wafer into strips such that measurements for both **longitudinal** (L) and **transversal** (T) cases were possible. Each case is defined by the direction of the stress (σ) relative to that of the current flow (J) (Figure 1).

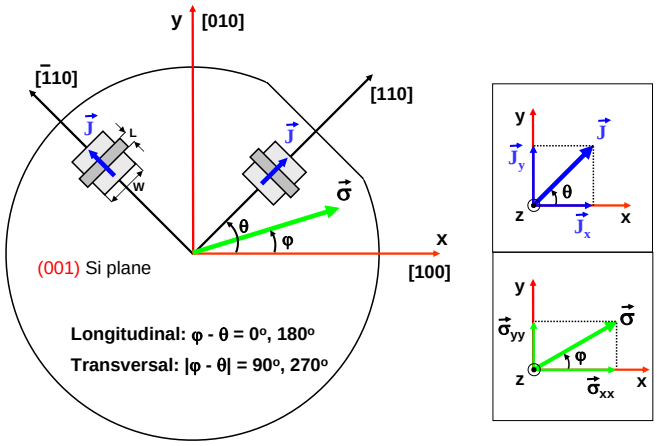

Fig. 1. Uniaxial stress direction relative to the MOS-FET current (**J**) flow

We measured long-channel (W x L) = (16 x 16) μm^2 and short-channel (W x L) = (16 x 0.8) μm^2 MOS-FETs. The measured devices have the gate oxide thickness $T_{ox} \approx 16$ nm. The measurements were performed at room temperature, using a HP4145 Semiconductor Parameter Analyzer.

B. Bending Method

To apply a constant and uniform uniaxial stress on the wafer strip we used the conventional 4-point bending technique [1] shown schematically in Figure 2.

Through this method we applied a known uniform uniaxial stress in the device under test (DUT). The calculated relation between the applied uniaxial stress and the deflection at the loads (V_L) and also details regarding our in-house built bending apparatus and the measurement techniques are provided in [2].

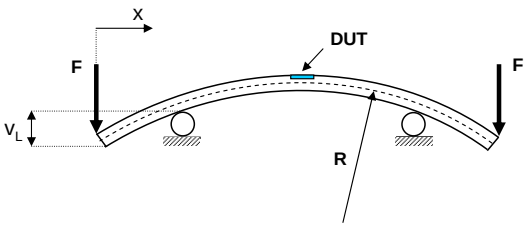

Fig. 2. The 4-point bending technique

III. Stress Effects on BSIM3 Parameters

The measurements performed on CMOS transistors in both longitudinal and transversal cases showed a significant variation in the drain current I_{DS} with the applied stress [2].

Accurate simulation of a transistor under stress can not anymore be achieved with the available BSIM3 parameter set for our $0.8\mu m$ CMOS process. This geometry-independent parameter set is used by a simulator like SPICE to predict the performance of any transistor in our CMOS process and is valid for zero stress only.

To simulate a MOS-FET under variable stress conditions, we need to identify and change those DC model parameters according to their sensitivity to an applied stress:

$$\Delta(parameter)/parameter = sensitivity \times stress \quad (1)$$

The changed BSIM3v3 parameter set will be stress dependent.

A. Extraction strategy

We investigated the parameters of the BSIM3v3 model that might be affected by the imposed uniaxial stress. The studied DC parameter groups were 1) the threshold voltage parameters and 2) the mobility parameters [3].

Using the IC-CAP device modeling software, we adjusted the standard global BSIM3v3 parameter set to the actual measured devices using Levenberg-Marquardt optimization. This procedure was repeated for each stress condition, for the selected parameters (e.g. VTH0, U0, VSAT, ETA0).

B. The threshold voltage parameter VTH0

One of the most important device parameters for modeling and circuit simulation is the threshold voltage (V_T). Additional to the parameter for long-channel device at zero substrate voltage VTH0, BSIM3 threshold voltage model contains other parameters describing the effects associated to non-uniform channel doping and scaling. VTH0 is determined by device physical parameters, such as the flat band voltage V_{FB}, bulk Fermi potential Φ_s and the body factor γ [3].

From MOS-FET input characteristics we extracted the values of VTH0, at different bending radius. The results presented in Figure 3 show that the threshold voltage is almost independent of stress $(< 0.5mV)$, in agreement with [4].

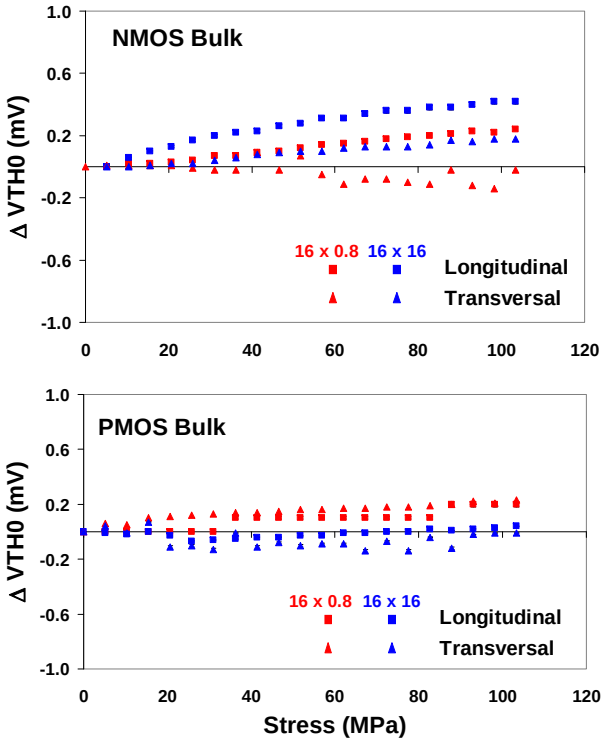

Fig. 3. Threshold voltage variation with applied uniaxial stress

C. The mobility parameter U0

Under the condition of negligible variations in the threshold voltage under the stress, the fractional change of the drain current I_{DS} is direct proportional to that of the effective mobility (μ_{eff}) and to the applied stress (σ) [4]:

$$\frac{\Delta I_{DS}}{I_{DS}} \cong \frac{\Delta \mu_{eff}}{\mu_{eff}} = \pi \cdot \sigma \quad (2)$$

π is the sensitivity of the drain current/mobility to the applied stress (Equation 1), known as the **piezoresistive coefficient**.

On one hand, π can be obtained directly from the measured variation of I_{DS} with the stress, but for short-channel MOSFETs, it must be corrected for the drain/source parasitic resistances (R_{DS}) [4]. On the other hand, using the extracted effective mobility variation with stress, π is corrected implicitly for R_{DS} in the extraction process.

In this work we use the carrier mobility BSIM3 model option MOBMOD=1 [3]:

$$\mu_{eff} = \frac{U0}{1 + (UA + UC \cdot V_{BS}) \cdot \frac{V_{GS}+V_T}{T_{ox}} + UB \cdot \left(\frac{V_{GS}+V_T}{T_{ox}}\right)^2} \quad (3)$$

where U0 is the zero-field mobility parameter and the parameters UA, UB and UC are fitting parameters that account for μ_{eff} degradation. In the first-order approximation we assume that the parameters UA, UB and UC are constant under the applied uniaxial stress.

Thus, we investigated the effect of stress only on U0. The results are depicted in Figure 4.

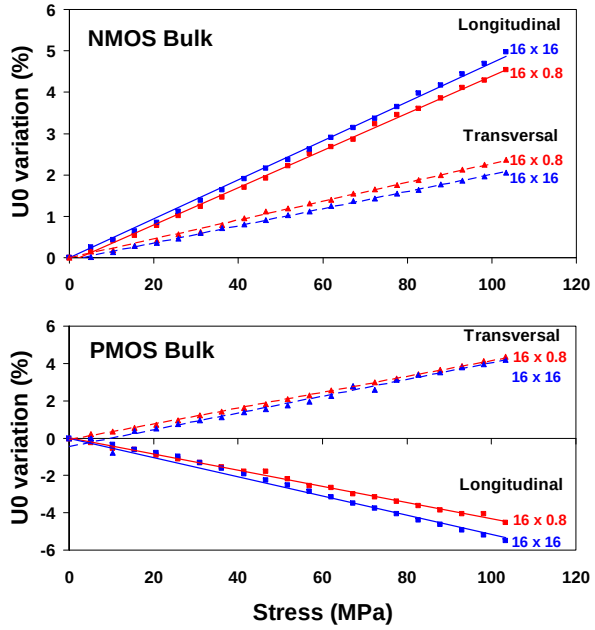

Fig. 4. Carriers mobility variation with applied uniaxial stress

The values of the piezoresistive coefficients (the slopes of the mobility variation with the applied uniaxial tensile stress) are listed in Table I.

Coeff.	$WxL = 16x0.8\ \mu m^2$		$WxL = 16x16 \mu m^2$	
	NMOS	PMOS	NMOS	PMOS
π_L	450	−440	470	−520
π_T	210	430	220	450
$\pi_S = \pi_L + \pi_T$	660	−10	690	−70
$\pi_{44} = \pi_L - \pi_T$	240	−870	250	−970
Error	±4%	±9%	±4%	±9%

TABLE I
PIEZORESISTIVE COEFFICIENTS FOR **BULK** MOS-FETS (x$10^{-12}\ Pa^{-1}$) ON (100) SILICON: π_L IS IN LONGITUDINAL CASE AND π_T IS IN TRANSVERSAL ONE (SEE FIGURE 1)

From Table I we notice that the values of the piezoresistive coefficient for the long-channel transistor are very similar to those of the short-channel one. This means that the MOS-FET channel sensitivity to the applied uniaxial stress is independent of the channel length, in accordance with [4], [5].

Other investigated also other parameters like the carriers saturation velocity VSAT and the threshold voltage drain induced barrier lowering parameter ETA0 presented small variations with the applied stress (VSAT$<2\%$ and ETA0$<0.5\%$).

IV. EXTENDED TRANSISTOR MODEL

In this chapter we introduce an extended MOS-FET circuit schematic that can be used to simulate the transistor under variable tensile/compressive uniaxial stress conditions.

To do that, we need a general relation of the piezoresistive coefficient π (Equation 2) for any stress application direction relative to the drain current flow direction on (001) Si plane.

A. General π Relation for (001) Silicon Plane

Based on the fundamentals of the piezoresistive effect [6], we derived a general expression for the piezoresistive coefficient on (001) silicon (Si) plane, for any direction of the current flow, defined by the angle θ and any stress application direction, defined by the angle φ (see Figure 1).

We started from the well-known relation between the electric field and the current density components:

$$\begin{bmatrix} E_x \\ E_y \end{bmatrix} = \begin{bmatrix} \rho + \Delta\rho_{xx} & \Delta\rho_{xy} \\ \Delta\rho_{xy} & \rho + \Delta\rho_{yy} \end{bmatrix} \cdot \begin{bmatrix} J_x \\ J_y \end{bmatrix} \quad (4)$$

where ρ is the isotropic resistivity of the unstressed crystal and $\Delta\rho_{ij}$ is its variation due to stress given by:

$$\Delta\rho_{ij} = \pi_{ijkl} \cdot \sigma_{kl}, \qquad (\forall) \quad i,j,k,l \in \{x,y\} \quad (5)$$

π_{ijkl} is the piezoresistive tensor and for the cubic Si crystal is determined by a set of three fundamental piezoresistive coefficients $\Pi = \{\pi_{11}, \pi_{12}, \pi_{44}\}$ [6], [7]. Each of them describes the fractional change in current induced by the applied stress, along $\{100\}$ silicon principal axis. π_{11} is the longitudinal coefficient ($(\varphi - \theta) = 0^o$) and π_{12} the transversal ($|\varphi - \theta| = 90^o$) one (see Figure 1). π_{44} is the shear coefficient, that together with π_{11} and π_{12}, determines the piezoresistive coefficient in any direction defined by $|\varphi - \theta| \in (0, 90)^o$.

The stress tensor components (Figure 1) for the plane stress condition (the stress effects in z direction are neglected) are:

$$\sigma_{kl} = \begin{bmatrix} \sigma_{xx} & \tau_{xy} \\ \tau_{yx} & \sigma_{yy} \end{bmatrix} \Rightarrow \sigma_{kl} = \sigma \cdot \begin{bmatrix} cos^2\varphi & cos\varphi \cdot sin\varphi \\ cos\varphi \cdot sin\varphi & sin^2\varphi \end{bmatrix} \quad (6)$$

σ_{kl} $(k = l)$ are the normal stresses and τ_{kl} $(k \neq l)$ are the shear stresses, calculated based on tensor rotation theory.

With Equation 5 and Equation 6 in Equation 4 we can write the final relation electric field-current density:

$$E = E_x \cdot cos\theta + E_y \cdot cos\theta \Rightarrow E = \rho(1 + \pi \cdot \sigma) \cdot J \quad (7)$$

Equation 7 gives us the **general** expression of the **piezoresistive coefficient** $\pi = \pi(\Pi, \theta, \varphi)$, in (001) Si plane, valid for any combination of angles (θ, φ).

$$\begin{aligned} \pi = \pi_{11} \cdot (cos^2\theta \cdot cos^2\varphi + sin^2\theta \cdot sin^2\varphi) \\ + \pi_{12} \cdot (cos^2\theta \cdot sin^2\varphi + sin^2\theta \cdot cos^2\varphi) \\ + 2\pi_{44} \cdot sin\theta \cdot cos\theta \cdot sin\varphi \cdot cos\varphi \end{aligned} \quad (8)$$

The fabricated transistors on (001) Si plane have the channel oriented such that the drain current flows in one of $\{110\}$ Si equivalent directions. In this case, $\theta = 45^o$ and $\theta = -45^o$. Equation 8 becomes:

$$\pi = \frac{\pi_{11} + \pi_{12}}{2} \pm \pi_{44} \cdot sin\varphi \cdot cos\varphi \quad (9)$$

where $\pi_{11} + \pi_{12} = \pi_S$ [4] that together with π_{44} are determined from measurements.

B. Proposed transistor model

The BSIM3 model for CMOS transistors has been modified by considering the mobility as the key parameter dependend on the applied stress. Now, Equation 2 can be written as:

$$\frac{\Delta I_{DS}}{I_{DS}} \cong \frac{\Delta U0}{U0} = \pm\pi(\Pi, \theta, \varphi) \cdot |\overrightarrow{\sigma}| \qquad (10)$$

The sign $+$ corresponds to the tensile uniaxial stress and the sign $-$ to the compressive one.

To simulate stress effects, we vary I_{DS} with a current controlled current source (**Fstress**), inserted in parallel to the MOS-FET (see Figure 5). The gain of the source **Fstress** is obtained by replacing Equation 9 and the stress $|\overrightarrow{\sigma}| = \sqrt{\sigma_{xx}^2 + \sigma_{yy}^2}$ (Figure 1) into Equation 10:

$$gain = \pm\left(\frac{\pi_S}{2} \cdot \sqrt{\sigma_{xx}^2 + \sigma_{yy}^2} + \pi_{44} \cdot \frac{\sigma_{xx} \cdot \sigma_{yy}}{\sqrt{\sigma_{xx}^2 + \sigma_{yy}^2}}\right) \qquad (11)$$

Equation 11 was translated into voltages, for SPICE simulator (see Figure 5.) σ_{xx} and σ_{yy} were translated into the voltages $V(Sx)$ and $V(Sy)$ based on the chosen convention $1MPa \Leftrightarrow 1V$. The sign $\pm$ is used for tension/compression.

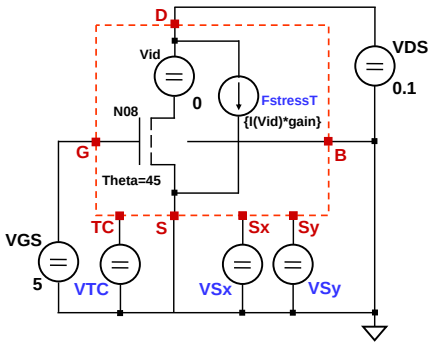

Fig. 5. The extended NMOS circuit for simulation of variable stress effects. The $\pm$ sign in the gain equation corresponds to the current flow direction given by $\theta = 45^o$ and $\theta = -45^o$. The voltages at S_x and S_y correspond to the stress components σ_{xx} and σ_{yy}. The voltage at TC, taking only the values ± 1, can switch between tensile (+1) and compressive (-1) stress.

V. Simulation Results

The stress dependent BSIM3 parameter set is validated with current mirror circuits, based on orthogonally oriented transistor pairs. The advantage of positioning the transistors in this way is that we could simulate both longitudinal and transversal cases simultaneously and compared them with the measured ones. Due to these orientations we have been able to observe in the same time the opposite behaviors of the MOS-FET pairs exposed to identical stress conditions. The simulation results (Figure 6) exhibit a good match with the measured data [8] for both NMOS and PMOS devices.

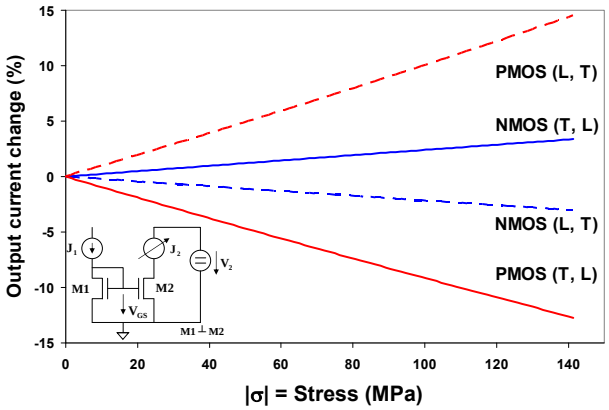

Fig. 6. The simulated drain current variation with stress in the N- and PMOS current mirror circuits where: $|\sigma_{xx}| = |\sigma_{yy}| = [0, 100]\ MPa$;
(L, T) stands for (M1 Longitudinal, M2 Transversal) and (T, L) for (M1 Transversal, M2 Longitudinal) (see Figure 1)

VI. Conclusion

In this work we presented part of an ongoing investigation on MOS-FETs and their BSIM3 model parameters under stress. We deduced a general relation for the piezoresistive coefficient used to extend the MOS-FET circuit, in order to include stress effects. For future work we intend to modify more BSIM3 model parameters according to their stress sensitivity. Moreover, we plan to extend our measurements to arbitrary stress application directions relative to the MOS-FET channel orientation and compare them to the simulation results. The case of the compressive uniaxial stress will also be considered.

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