Accurate Measurement of Piezocoefficients in CMOS Transistors on Conventional and Ultra-Thin Silicon Chips

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***Abstract*—With the ongoing miniaturization and integration, flexible electronics become more and more important. However, deformation introduces stress that must be considered in the measurement procedure, to obtain accurate and repeatable measurements. In this paper we focus on measurement methods for thin-film and bulk transistors under stress conditions and compare them. We present the used bending principles and the corresponding build apparatus. The obtained results underline the importance of choosing a reliable electrical connection method to device under test.**

***Index Terms*—Bending, flexible electronics, piezoresistivity, strained-Si, uniaxial stress.**

I. Introduction

Technological advances in the production of integrated circuits (IC's) enable a variety of new application domains such as retina implants, electronic paper or intelligent textiles. While chips in the past have been bulky and solid, these new production methods allow for very thin chips with the potential to bend and twist.

Deformation leads to the so-called piezoresistive effect, which needs to be considered in circuit design. The applied mechanical stress induces strain in the silicon chips, changing the crystal electronic properties. Hence, the electrical characteristics of CMOS transistors are affected by the applied stress. Therefore, the transistor characteristics will no longer be static but vary with the applied stress. To characterize this piezoresistive effect we need to accurately determine values for longitudinal and transversal piezocoefficients. To do so, accurate measurements of transistors characteristics under different stress conditions are needed.

The objective of this paper is twofold: First we present the adopted bending methods and the used apparatus to induce a uniform uniaxial stress in both conventional and thin-film transistors. The second objective is the analysis and our experiences with the two methods used to contact the device under test (DUT): adjustable probes and bond-wired connections.

The paper is structured as follows: in Section II we are going to introduce the measured transistors and contacting methods. Further we discuss the adopted bending principles and apparatus. Section III brings into attention our results with each contacting method and our observations in order to get accurately and repeatable measurements. Finally, we conclude this paper in Section IV with a brief conclusion and ideas for future work.

II. Experiments

A. Tested Devices

We fabricated CMOS transistors on ultra-thin ($20\mu m$) silicon chips by using Chipfilm^{TM}technology [1] and bulk transistors, for comparison. Both thin-film and bulk chips were processed in parallel using an in-house IMS $0.8\mu m$ CMOS process.

After the fabrication of the thin-film chips, we broke them off the wafer by the Pick, Crack&Place^{TM}method [1] and mounted on polyimide foil. The chips were attached to substrate in two positions. This made possible the application of stress both longitudinal and transversal to the MOS channel orientation.

For measurements on the bulk chips we sawed the wafer into strips along the $[110]$ and $[\bar{1}10]$ crystallographic directions. Hence, measurements for longitudinal and transversal applied stress were possible. The strip was about $130\ mm$ long and $15\ mm$ wide. Each case was defined by the direction of the stress (σ) relative to that of the current flow (J) . To measure the

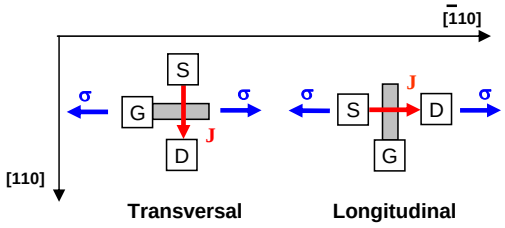


Fig. 1. Applied stress direction relative to MOS-FET channel orientation

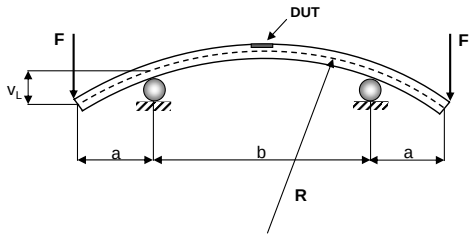
DC characteristics, we chose a long-channel MOS transistor (Width x Length) μm^2 = (16 x 16) μm^2. The channel was oriented such that the flow of current was in the $[110]$ and $[\bar{1}10]$, on the plane (100). The measurements were performed at room temperature, using an HP4145 Semiconductor Parameter Analyzer.

B. Bending Methods

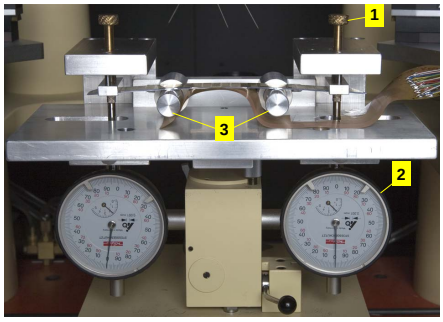
In the following we present our methods for measuring our bulk and thin-film transistors. We do so by describing

the electrical contacting method, the bending principle and apparatus used for achieving the measurements.

1) Bulk chips: Wafer strips were exposed to mechanical stress by using a conventional 4-point bending method [2]-[3]. The schematic of the loading fixture is shown in Figure 2a.



(a)



(b)

Fig. 2. (a) 4-point bending technique, (b) Bending apparatus

The decisive factor for the bending method to be used was to get a constant stress in the wafer strip, where the DUT is located.

Calculations based on the beam bending theory ([4], [5]) show a constant bending moment within the region specified by the dimension b (see Figure 2a). This stress at the top surface in the bending direction can be expressed as function of the bending radius R or, in our case, of the measured deflection at loads:

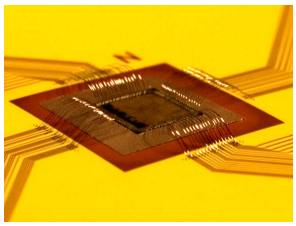
$$\sigma_1 = E \cdot \frac{h}{2R} \Leftrightarrow \sigma_1 = E \cdot \frac{3h}{a(2a+3b)} v_L \qquad (1)$$

where E stays for modulus of elasticity of the material (Si) and h for the beam's thickness.

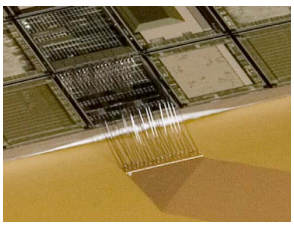
In order to conduct the bending experiment, an in-house bending apparatus was built (Figure 2b). The controlled deflection at the ends of the strip was done with two precision screws (1) and two mechanical displacement gauges (2). Based on calculations, the stress is applied uniformly between the two cylindrical supports (3). Hence we aligned the wafer strip such that the DUT was located there.

Before starting measurements, the apparatus was calibrated and additionally a preliminary mechanical breaking test was performed. The test showed a breaking point for the wafer strip around $170 - 200\ MPa$. That is in accordance with previous work [2], [6]. Therefore, to avoid fracture, we kept the applied stress below $120\ MPa$ ($R \simeq 50\ cm$).

2) Thin-film chips: After fabrication, thin-film chips were broken off the wafer and assembled by Pick, Crack&Place^{TM}process [1]. After that we glued the thin chip on a $50\mu m$ thick Kapton® polyimide foil. The pads of the chip were bond-wired to electrical leads already present on the substrate and distributed around the chip as is shown in Figure 3a.



(a)

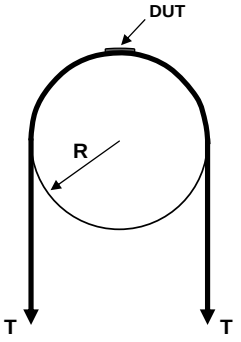


(b)

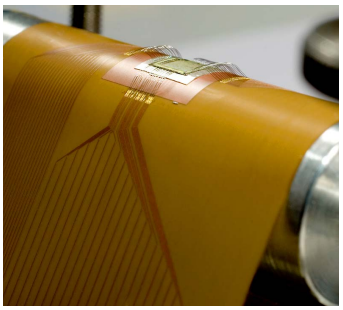
Fig. 3. Bond-wired electrical connection
(a) Thin-film chip (b) Bulk transistor

Bond-wired connection it is known [7], [8] as a good contacting method between the CMOS circuits on the chip and the external electronics. Combining the brittle device material with a compliant elastomeric substrate made possible its handling in mechanical deformation.

To study the electrical behavior of thin-film transistors (TFTs) under mechanical stress, the thin-film chip/substrate was wrapped around cylinders of well-defined radii, as presented schematically in Figure 4a. The implemented bending is depicted in Figure 4b, showing a part of the build in-house bending apparatus.



(a)



(b)

Fig. 4. Thin-film chip bending
(a) The principle: thin-film DUT on foil bent under defined radii (R), (b) Apparatus: cylindrical deformation

This apparatus was used to enforce a well-defined bending radius onto the chips on tape thus applying a defined level of tensile stress to the DUT. The minimum radius we have used was $R = 10\ mm$ corresponding to a stress in the DUT of $\sim 200\ MPa$.

The stress was calculated based on the following relation:

$$\sigma_2 = E_c \cdot \frac{1}{2R} \cdot \frac{E_c h_c^2 + E_s h_s (2h_c + h_s)}{E_c h_c + E_s h_s} \qquad (2)$$

where R is the bending radius, $h_c = 20\ \mu m$ the chip thickness, $h_s = 50\ \mu m$ the substrate thickness and $E_c \simeq 170\ GPa$, $E_s = 5.37\ GPa$ are the elastic moduli of the chip and of the substrate. Details about this formula can be found in [9].

III. Analysis

The electrical behavior of CMOS transistors under stress is well known ([10]-[11]). On one hand, the NMOS drain current increases under tensile stress in both cases longitudinal and transversal. For PMOS, on the other hand, the drain current increases only in transversal case but decreases in longitudinal one. These phenomena were attributed to energy-level change in the valence band caused by external stress [12]-[13].

In order to study the piezoresistive behavior of MOS transistors, two types of connections have been used: the first one by using **adjustable probes** and the second one by using **bond-wired connections**. The quality of measured data e.g. accuracy and repeatability is that we need to be aware when we chose the type of contact.

We started measurements on NMOS bulk transistors, with adjustable probes. The applied tensile stress was transversal to the drain current flow. From results, we extracted the values of the drain current in linear (at $V_D = 100\ mV$) and in saturation (at $V_D = 5\ V$), at different curvature radius. With these values we calculated the percentage change in the drain current relative to stress-free state. These results are graphically represented in Figure 5.

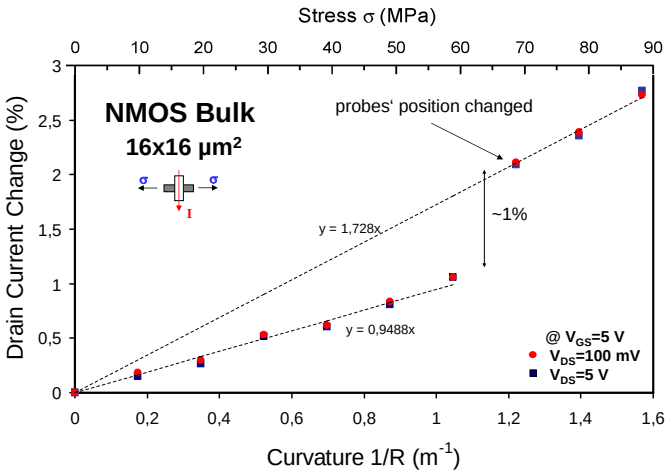


Fig. 5. Adjustable probes: percentage change of drain current with curvature

As expected, the drain current increases linearly with curvature/stress. However, between the seventh and the eighth measurement a disruption in the linearity of the measurement can be noticed. This discontinuity can be observed at a curvature of $\sim 1.2\ m^{-1}$ ($R \simeq 80\ cm$) and corresponds to $\sim 1\%$ drain current shift.

Hence the first seven measurements lead to a different gradient than the last three ($\sim 80\%$ difference in the slopes). Our analysis of this phenomenon revealed that this disruption occurs exactly when the probes' tips where moved to a different point on the transistor's pads. We repeated the measurement several times to verify our assumption which proofed to be correct.

When measuring devices on wafers without bending, it is usually not necessary to move the probes during a single series of measurements. Unfortunately, this is not the case when measuring bent devices. At every increase in curvature, the probes had to be removed from contacts and afterwards brought back again. That was necessary to avoid higher pressure on transistor's pads or to damage the needle's tip. We suspected that this removing and reconnecting step was the reason behind the discontinuity in our measurement as shown in Figure 5.

One can notice a variation of $\sim 80\%$ between the two slopes.

To verify our suspicion, we did another series of measurements on the same NMOS bulk transistor. This time, the wafer strip was maintained flat during the measurements. The transistor's pads were probed in three different points. For each position, 10 successive measurements were accomplished. The results are presented in Figure 6.

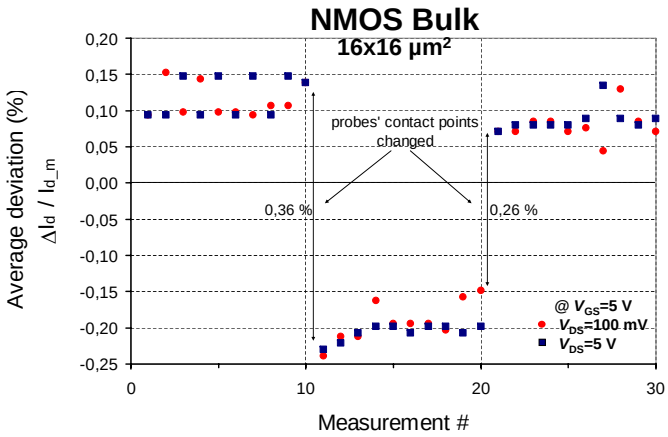


Fig. 6. Measurement accuracy verification

After the first 10 measurements we changed the contact position of probes. Results show a deviation of the drain current of 0.36% from an average value I_{d_m}. At the second change of probes' positions, a difference of 0.26% was noticed.

We put the explanation of these differences in measurements on variation of the electrical contact resistance between the prober and the probe, in our case between the needles and the transistor's pads. This problematic is not new and was largely discussed in literature [14], [15].

Based on these results, we concluded that the measurements with adjustable probes are not the perfect choice for our piezoresistive investigations because they generate not enough accurate and reproducible results.

Hence, we changed the contacting procedure for bulk transistors. This time, each DUT's pad was wired to a flexible printed circuit on Kapton® foil, as shown in Figure 3b.

We used the same bending device (see Figure 2b) to generate the required uniaxial loadings. Similar measurement

conditions were preserved in order to verify that the electrical contact type has indeed an impact on the accuracy of measurements. The results are depicted in Figure 7.

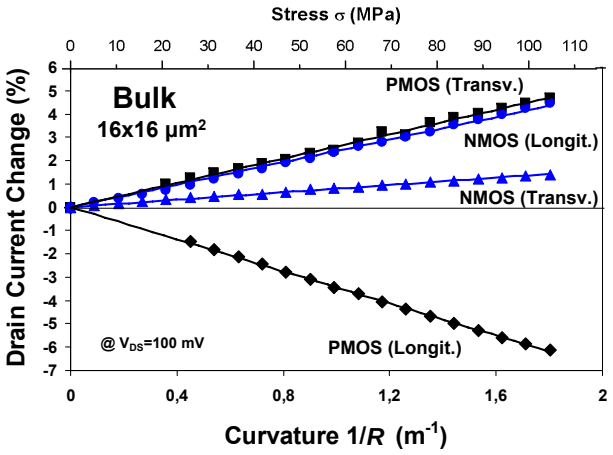


Fig. 7. Results (at $V_{ds} = 100mV$) with bond-wired connections on bulk NMOS and PMOS transistors with channel oriented longitudinal and transversal to tensile applied stress

For the same stress value, the graph shows an increase of about 5% in NMOS drain current for longitudinal case compared with just ∼1.4% for transversal case. Unlike the results for NMOS transistor under stress, in case of the PMOS transistor the drain current decreases with about 6% when applying longitudinal stress. The graph shows an increase of about 4% in drain current when the PMOS channel is oriented transversal to applied stress. These results are in good agreement with previous results from literature [2], [11], [16].

We repeated the measurements three times and the measured data sets were inline one each other. This confirmed us that using bond-wired connections to DUT was a good choice in bending measurements and will be used in further investigations.

The effective values of piezoresistive coefficients were extracted from the slopes of the drain current variation with stress. Their values expressed in Pa^{-1} are listed in Table I together with other results from literature ([2]), for comparison.

Coeff.	**Our results** $WxL = 16x16\ \mu m^2$		Gallon & al. [2] $WxL = 10x10\mu m^2$		Bradley & al. [6] TI: $L = 16\mu m$	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
π_L	478	−637	485	−600	320	−415
π_T	134	409	212	383	250	385
Error			$\sim \pm 60x10^{-12}\ Pa^{-1}$		not given	

TABLE I
PIEZORESISTIVE COEFFICIENTS FOR **BULK** MOS-FETS ($x10^{-12}\ Pa^{-1}$) ON (100) SILICON: π_L IS THE LONGITUDINAL PIEZOCOEFFICIENT AND π_T IS THE TRANSVERSAL ONE

The estimated error in the piezoresistive coefficients is composed of the errors in measurements and in calculations. The error analysis will be included in a future paper.

IV. Conclusion

Many factors influence the performance of measurements like the measurement conditions or the precision of the experimental setup. With this work we faced another important factor that should be considered in bending measurements: the electrical contact method to the DUT. The results demonstrated its importance in obtaining accurate and repeatable measured data.

This work is only the first part of an ongoing investigation in MOS-FETs under stress. For future work we are going to perform further experimental measurements on transistors with varying gate dimensions. Moreover, we plan to extend our analysis and measurements to arbitrary stress application directions relative to the MOS-FET channel orientation.

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