A Seamless Ultra-Thin Chip Fabrication and Assembly Process

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Introduction - Various new applications of silicon technology, such as 3D circuit integration [1], system-on-chip (SoC), system-in-package (SiP), and electronics on foil or textile [2], call for low-cost manufacturing and assembly of ultra-thin chips (5-50 μm). Practically all currently pursued concepts for fabricating thin chips are based on post-process thinning at wafer level, which, at thickness <50 μm, require application of a costly handle substrate. Also, grinding techniques applied to very thin wafers may lead to defect formation, thickness non-uniformity (wedging), and wafer fracture, thus causing yield loss and leading to high cost at this late stage of manufacture [3]. We propose a new concept based on thin-chip fabrication by wafer pre-processing prior to the CMOS integration instead of post-process thinning of the entire wafer. There, the conventional chip dicing is replaced by a novel Pick, Crack & Place™ process, through which the thin chip fabrication and assembly processes are seamlessly connected (Fig. 1).

Pre-process formation of ultra-thin chips – In the new technology the chip thickness is defined in pre-processing [4] by forming a buried cavity beneath the wafer surface within the chip areas. Two processes have been developed to achieve this goal (Fig. 2a,b). In both cases the buried cavities are created by a local porous silicon formation (A3, B3) on heavily doped p-type substrates (0.014 Ω-cm) followed by an annealing step at 1100 °C for 30 minutes (A4, B4) and an epitaxial film deposition at 1100 °C in $SiHCl_3$ at 760 Torr (A5, B 5). While in Process A the thin-chip areas are defined by using a 100-nm thick nitride mask layer (A2) the more advanced Process B uses a heavy n-type implant (P, 10^{15} cm^{-2}) to define regions, in which no anodization takes place (B2). As a consequence of the nitride mask the epitaxial growth results in an epi/poly co-deposition (A5) leading to a distinct surface topography ("Process A" in Fig. 3). In contrast, the implant mask allows for achieving a perfectly planar epitaxial overgrowth so that the pre-processed wafers can be handled in the CMOS fabrication like any conventional wafer substrate ("Process B" in Fig. 3). While with Process A direct photolithographic alignment can be used (see Fig. 2, A5, and Fig. 3), though with difficulties in photoresist spin-on, sufficiently accurate global wafer flat alignment is used for wafers from Process B. The porous silicon layer is formed through anodic etching [2],[5],[6] resulting in a stack of fine and coarse porous silicon (Fig. 4a). During the annealing the coarse layer transforms into a continuous 200-nm high cavity that separates the 'chip-to-be' from the substrate (Fig. 4b). In spite of the high annealing and epitaxial growth temperature autodoping from the heavily doped substrate is sufficiently low (Fig. 5).

Pick, Crack & Place™ process - While during the CMOS processing steps the chips are attached to the substrate along the entire perimeter (see Figs. 1a), trenches are etched subsequently to free the chips leaving only anchor points at the corners (Fig. 1b,c; Fig. 6a) or at the sides (Fig. 6b). Those anchors are designed to keep the chips attached to the substrate during the final wafer handling but allow for cracking off and transferring the chips by using a conventional pick&place tool (Fig. 7). These two process modules are the only steps carried out after CMOS fabrication, thus minimizing costly yield loss. Fig. 8 shows the wafer after removal of 22-μm thick chips, indicating the feasibility of the Pick, Crack & Place™ process.

Characterization - Device test structures and a bitprocessor chip (30,000 transistors; 16 MHz) were fabricated in a CECC certified 0.8-μm CMOS manufacturing process at IMS CHIPS (Fig. 8). These test devices and circuits had been fabricated on wafers including chips with the buried cavity in the center part of the wafers as well as chips elsewhere, only having the epi-film and thus serving as controls. Figs. 10a,b and 11a,b show that the on-wafer distributions of the carrier mobilities of NMOS (Fig. 10a) and PMOS (Fig. 10b) transistors, as well as the as-measured (Fig. 11a) and channel-length variation adjusted (Fig. 11b) frequencies of CMOS ring oscillators exhibit no difference between chips with and without the buried cavity. Only the p-well/n-epi leakage current density was slightly higher as a result of the porous silicon layer at the chip's backside, though meeting the specifications of the manufacturing process. For the bitprocessor fabricated on both types of chips nearly identical, high yield figures were found, indicating that the epitaxial film growth on the epi-overgrown porous silicon chip regions reaches a film quality that is very comparable to that on the controls. Moreover, Fig. 12 illustrates the excellent mechanical stability of the chips, indicating that they can easily be mounted onto non-planar surfaces and flexible foil.

Conclusions - In can be concluded that the new thin-chip fabrication process is feasible and presents a unique alternative to the currently established post-process wafer thinning techniques for fabricating ultra-thin silicon chips. In particular, the wafer pre-process approach allows for low-cost fabrication of thin chips and the very accurate thickness control of ultra-thin chips with known good yield provides new possibilities for 3D chip stacking technologies. A general advantage is that the ultra-thin and flexible chips are mechanically supported at all stages of the chip fabrication and assembly process.

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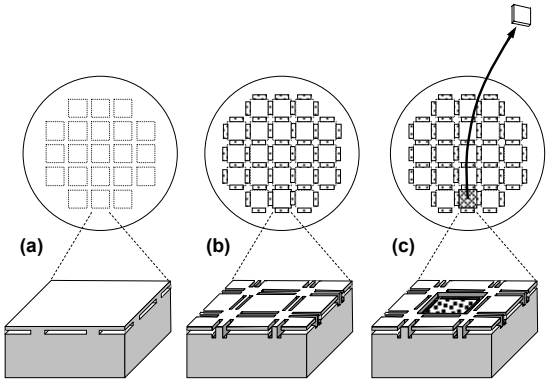


Fig. 1 Schematic illustration of the new Pick, Crack & Place™ process with (a) the pre-process buried cavity and strong chip attachment, (b) after trench etching to reach a weak chip attachment, and (c) after chip detachment.

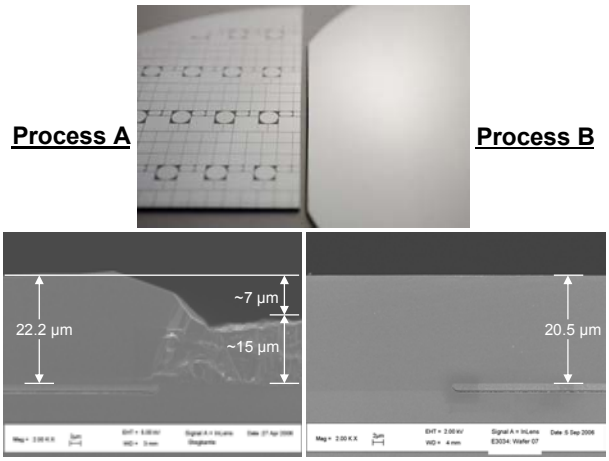


Fig. 3 Comparison of plan views (top) and of cross-sectional SEM's of the pre-processed wafers at the transition from chip area to the chip divider (bottom) for Process A featuring a pronounced surface topography from the 22/15-µm epi/poly co-deposition (left) and Process B having a perfectly planar surface (chip thickness = 20.5 µm epi + 1.5 µm annealed porous silicon = 22 µm) from using an implant mask for the local porous silicon formation (right).

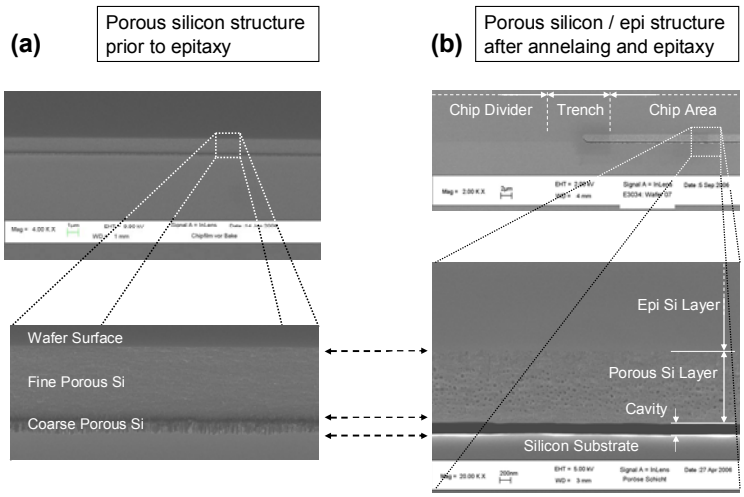


Fig. 4 Cross-sectional SEM of the chip area (a) before and (b) after anneal and epitaxial overgrowth of the fine/coarse porous silicon film that transforms into a 200-nm high buried cavity residing 22 µm beneath the wafer surface (Process B).

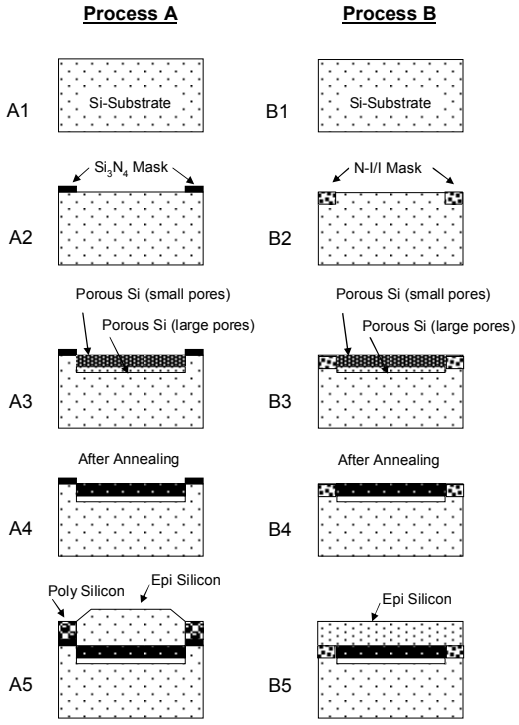


Fig. 2 Flows of two different processes for the fabrication of ultra-thin chips using either a nitride mask and epi/poly co-deposition (Process A) or an implant mask followed by a uniform planar epitaxial film deposition (Process B).

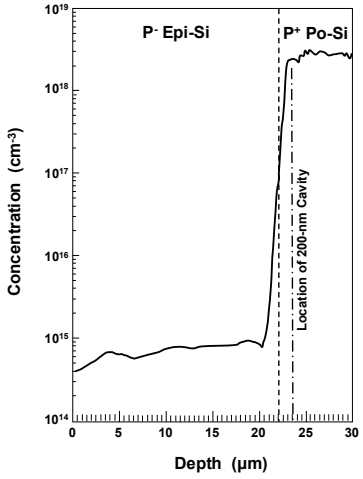
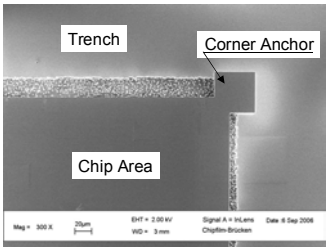
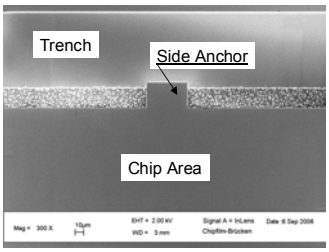


Fig. 5 Doping concentration of a test sample (epi n-type doping turned off) having a 22-µm thick p^- epi layer, a 1.3-µm fine-porous silicon layer, and a 200-nm cavity over a p^+ substrate from spreading resistance measurement. Note, that the signature of the cavity is only barely visible due to the large radius (>0.5 µm) of the probes.



(a)



(b)

Fig. 6 Plan view photographs of chips prior to the detachment by Pick, Crack & Place™ having anchor points at the corners (a) or at the sides (b).

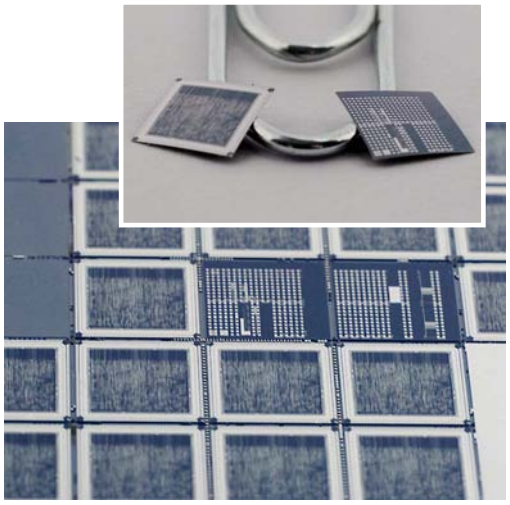


Fig. 8 Photo of a section of the wafer where rectangular test chips and microprocessor chips (each 5x5 mm^2) have been removed by Pick, Crack & Place™. These detached two chips are shown in the insert.

Fig. 12 Photo of a clamped chip illustrating the excellent mechanical stability and flexibility of the 22-µm thin chips.

Fig. 7 Snapshots from a video illustrating the Pick, Crack & Place™ process.

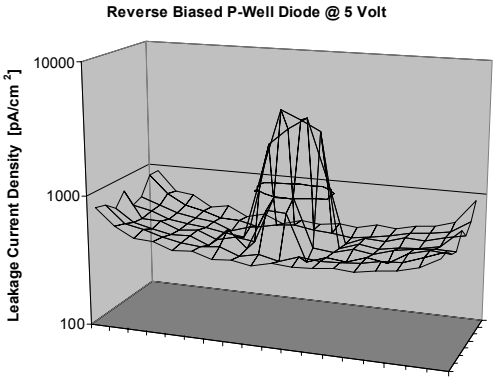


Fig. 9 Reverse leakage current densities of p-well/n-epi diodes measured across a strip of chips on circuit product wafers having chips with cavities from porous silicon formation underneath in the center part and chips without cavities elsewhere. As a result the chips with cavities underneath had leakage current densities that were only less than 10x higher than that of the controls, indicating that the trap density was only 10x-100x higher. Note, that all measured current densities met the specifications of this particular product.

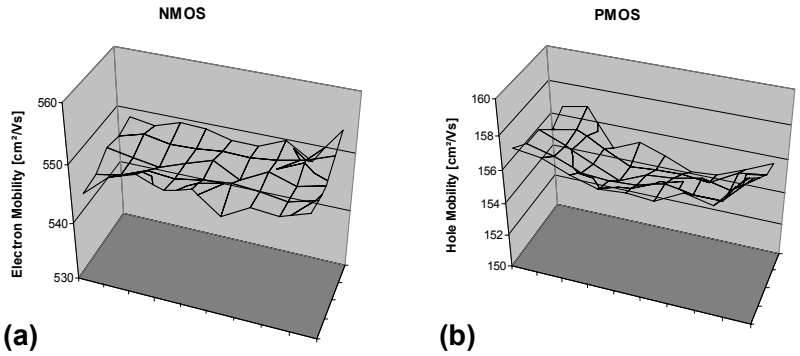


Fig. 10 Extracted electron and hole mobilities of (a) NMOS and (b) PMOS transistors, respectively, across a test region with and without buried cavities (see also caption of Fig. 9).

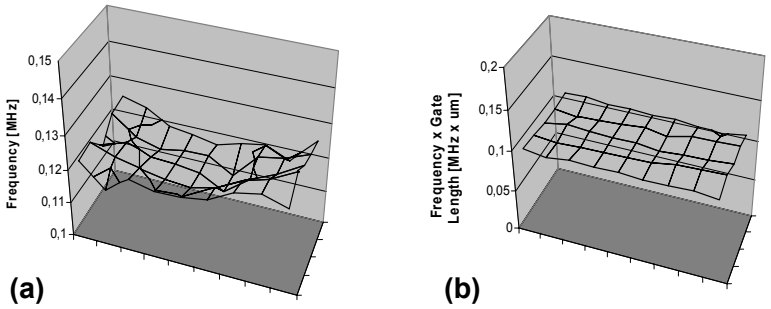


Fig. 11 Frequencies (a) and gate-length adjusted frequencies (b) of 148-stage CMOS ring oscillators with a subsequent 5-stage divider measured across a test region including chips with and without buried cavities (see also caption of Fig. 9).